VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification

The paragraph at page 13, line 28 to page 14, line 2 has been amended as follows:

FIG. 5C is an enlarged plan view of encircled detail 5C in FIG. 5A that shows a representative pad 116 and metal trace 144 in greater detail. Since pad 116 and metal trace 144 are not ~~be~~ visible from surface 114 of chip 110, they are shown in phantom. Metal trace 144 includes a distal end that overlaps pad 116.

The paragraph at page 21, lines 8-17 has been amended as follows:

At this stage, device 186 includes chip 110, conductive traces 150, transparent adhesive 154, connection joints 180 and insulative housing 184. Conductive traces 150 each include a lead 138 that protrudes laterally from **and** extends through a side surface 162 of insulative housing 184, and a metal trace 144 within insulative housing 184 that contacts an associated lead 138 and connection joint 180. Conductive traces 150 are electrically connected to pads 116 by connection joints 180 in one-to-one relation, and are electrically isolated from one another. Leads 138 are arranged in opposing rows that protrude laterally from and extend through opposing side surfaces 162 and are disposed between top surface 164 and bottom surface 160. Furthermore, light sensitive cell 115 is protected by and exposed to incident light from the external environment by transparent adhesive 154 and transparent base 182.

The paragraph at page 26, lines 4-22 has been amended as follows:

The connection joints can be formed from a wide variety of materials including copper, gold, nickel, palladium, tin, alloys thereof, and combinations thereof, can be formed by a wide variety of processes including electroplating, electroless plating, ball bonding, solder reflowing and conductive adhesive curing, and can have a wide variety of shapes **and** ~~as~~ sizes. The shape and composition of the connection joints depends on the composition of the conductive traces as well as design and reliability considerations. Further details regarding an electroplated connection joint are disclosed in U.S. Application Serial No. 09/865,367 filed May 24, 2001 by

Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electroplated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding an electrolessly plated connection joint are disclosed in U.S. Application Serial No. 09/864,555 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" which is incorporated by reference. Further details regarding a ball bond connection joint are disclosed in U.S. Application Serial No. 09/864,773 filed May 24, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Ball Bond Connection Joint" which is incorporated by reference. Further details regarding a solder or conductive adhesive connection joint are disclosed in U.S. Application Serial No. 09/927,216 filed August 10, 2001 by Charles W.C. Lin entitled "Semiconductor Chip Assembly with Hardened Connection Joint" which is incorporated by reference.

REMARKS

I. RESTRICTION REQUIREMENT

The Examiner asserts that the application contains claims directed to the following patentably distinct species:

Species	Figures
I	5A-5C
II	6A-6D
III	7A-7D
IV	8A-8E
V	9A-9B
VI	10A-10E
VII	12A-12C

The Examiner requires that Applicant elect a single disclosed species for prosecution on the merits and include an identification of the species that is elected consonant with this requirement and a listing of all claims readable thereon.

Applicant provisionally elects species VII (Figures 12A-12C) and claims 1-60 for prosecution on the merits. Applicant also traverses the restriction requirement and requests that it be withdrawn.

Claims 1-60 are directed to an optoelectronic semiconductor package device that includes (1) a semiconductor chip that includes a light sensitive cell and a conductive pad, (2) an insulative housing that includes a transparent housing portion, and (3) a conductive trace that is electrically connected to the pad.

The restriction requirement is flawed for several reasons.

First, the Examiner has mischaracterized the claims.

FIGS. 1A-14A and 1B-14B are bottom and top perspective views, respectively, of a method of making an optoelectronic semiconductor package device in accordance with an embodiment of the present invention.

In FIGS. 11A and 11B, pads 116 are electrically connected to metal traces 144 by connection joints 180. Likewise, in FIGS. 1A-10A and 1B-10B, pads 116 have yet to be electrically connected to and are electrically isolated from metal traces 144.

Independent claims 1, 11, 21, 31, 41 and 51 recite a conductive trace that is electrically connected to a pad.

Therefore, the Examiner's assertion that the application contains claims directed to species I-VI is clearly erroneous.

Second, Examiner has not even attempted to explain how examining species I-VII would involve separate classification, separate status in the art, or a different field of search (M.P.E.P. § 808.02).

There must be a serious burden on the Examiner if the restriction is required (M.P.E.P. § 803). Where the related inventions as claimed are shown to be distinct, the Examiner, in order to establish reasons for insisting upon restriction, must show by appropriate explanation one of the following: (A) separate classification thereof; (B) a separate status in the art when they are classifiable together; or (C) a different field of search (M.P.E.P. § 808.02).

Therefore, the Examiner has ignored mandatory elements set forth in the M.P.E.P. and the restriction requirement is improper.

II. AMENDMENTS

The Specification has been amended to improve clarity. No new matter has been added.

III. CONCLUSION

In view of the remarks set forth herein, the application is believed to be in condition for allowance. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 24, 2002.

D Sigmond — 12/24/02

David M. Sigmond
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Date of Signature

Respectfully submitted,

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